

**Bump Site Transfer and Qualification of Select 6L and 8L SOT23
Flip Chip on Lead Packages**

**Automotive Qualification Plan Summary for
6-SOT_23 at CARSEM**

TEST	SPECIFICATION	SAMPLE SIZE	EXPECTED COMPLETION DATE
Temperature Cycle (TC)*	JEDEC <i>JESD22-A104</i>	3 x 77	Sept 2018
Solder Heat Resistance (SHR)*	JEDEC/IPC <i>J-STD-020</i>	3 x 11	Sept 2018
High Temperature Storage Test (HTS)	JEDEC <i>JESD22-A103</i>	1 x 77	Sept 2018
Temperature, Humidity and Bias Test (THB)*	JEDEC <i>JESD22-A101</i>	3 x 77	Sept 2018
Unbiased Highly Accelerated Stress Test (UHAST)*	JEDEC <i>JESD22-A118</i>	3 x 77	Sept 2018
Electrostatic Discharge <i>Field Induced Charge Device Model</i>	ANSI/ESDA/JEDEC <i>JS-002</i>	3/voltage	Sept 2018

* These samples will be subjected to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: 1. Bake – 24 hours at 125°C; 2. Soak – unbiased soak for 192 hours at 30°C, 60%RH; 3. Reflow – three passes through a reflow oven with a peak temperature of 260°C. TC samples will be subjected to wire-pull test after 500 cycles where results should be within specification limits.

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High Temperature Storage (HTS)	JEDEC <i>JESD22-A103</i>	1 x 77	Sept 2018
Electrostatic Discharge <i>Field Induced Charge Device Model</i>	ANSI/ESDA/JEDEC <i>JS-002-2014</i>	3/voltage	Sept 2018

* Preconditioned per JEDEEC/IPC J-STD0020.

PCN 18_0064

PCN Title: Bump Site Transfer and Qualification of Select 6L and 8L SOT23 Flip Chip on Lead Packages

Change Items	From	To
Bumping Site	Amkor Taiwan (AT5)	Chipbond, Taiwan (CB4)
Die Level Bumping	High Lead Bumping	Cu Pillar/SnAg Bumping
Assembly	High Lead bumped die Flip Chip on Lead assembly with Solder Screen Printing on leadframe step before Flip Chip attachment on leadframe	Cu Pillar/SnAg bumped die Flip Chip on Lead assembly process where the Solder Screen Printing on leadframe step is replaced with Flux Dip step before Flip Chip attachment on the leadframe